

WHAT IS CLAIMED IS:

1. A phase-error suppressor for use with a plurality of
2 transistors having a common source coupled to a current generator
3 and configured to receive signals at a frequency, comprising:
4 an inductor, coupled between said common source and said
5 current generator, configured to resonate proportionally to said
6 frequency with a first capacitance associated with said plurality
7 of transistors.

2. The phase-error suppressor as recited in Claim 1 wherein
1 said plurality of transistors and said current generator form a
3 portion of a system selected from the group consisting of:
4 a quadrature oscillator buffer,
5 a quadrature oscillator, and
6 a quadrature mixer.

3. The phase-error suppressor as recited in Claim 1 wherein
2 said inductor and said first capacitance resonate at twice said
3 frequency.

4. The phase-error suppressor as recited in Claim 1 wherein
2 said first capacitance is dominated by a base-to-emitter
3 capacitance of at least one of said plurality of transistors.

5. The phase-error suppressor as recited in Claim 1 further
2 comprising a capacitor coupled to said inductor and coupled in
3 parallel to said current generator, said capacitor being configured
4 to shunt said inductor to ground at a selected radio frequency
5 (RF) .

6. The phase-error suppressor as recited in Claim 1 wherein
2 said frequency is at least three GHz.

7. The phase-error suppressor as recited in Claim 1 where
2 said signals are four periodic local oscillator signals having a 90
3 degree phase difference.

8. A method of suppressing a phase-error for use with a
2 plurality of transistors having a common source coupled to a
3 current generator and configured to receive signals at a frequency,
4 comprising:

5 coupling an inductor in series between said common source and
6 said current generator; and

7 causing said inductor to resonate proportionally at said
8 frequency with a first capacitance associated with said plurality
9 of transistors thereby suppressing a phase-error associated with
10 said signals.

9. The method as recited in Claim 8 wherein said plurality
2 of transistors and said current generator form a portion of a
3 system selected from the group consisting of:

4 a quadrature oscillator buffer,
5 a quadrature oscillator, and
6 a quadrature mixer.

10. The method as recited in Claim 8 wherein said inductor
2 and said first capacitance resonate at twice said frequency.

11. The method as recited in Claim 8 wherein said first
2 capacitance is dominated by a gate-to-source capacitance of said
3 transistors.

12. The method as recited in Claim 8 further comprising
2 coupling a capacitor to said inductor and in parallel to said
3 current generator, said capacitor shunting said inductor to ground
4 at a selected radio frequency (RF) .

13. The method as recited in Claim 8 wherein said frequency
2 is at least three GHz.

14. The method as recited in Claim 1 wherein said signals are
2 four periodic local oscillator signals having a 90 degree phase
3 difference.

15. An image-rejecting down-converter for use with a radio
2 frequency (RF) receiver, comprising:

3 a local oscillator (LO) configured to provide an in-phase
4 signal and a quadrature-phase signal at a frequency;

5 a quadrature mixer configured to combine said in-phase and
6 said quadrature-phase signals with a RF signal; and

7 a quadrature oscillator buffer, coupled between said LO and
8 said quadrature mixer, including:

9 a plurality of transistors having a common source coupled
10 to a current generator and configured to receive one of said
11 in-phase and said quadrature-phase signals from said LO at
12 said frequency; and

13 an inductor, coupled between said common source and said
14 current generator configured to resonate proportionally to
15 said frequency with a first capacitance associated with said
16 plurality of transistors to suppress a phase-error between
17 said in-phase and said quadrature-phase signals.

16. The image rejecting down-converter as recited in Claim 15
2 wherein said quadrature mixer, includes:

3 a second plurality of transistors having a second common
4 source coupled to a second current generator and configured to
5 receive one of said in-phase and said quadrature-phase signals at
6 said frequency; and

7 a second inductor, coupled between said second common source
8 and said second current generator, configured to resonate
9 proportionally to said frequency with a second capacitance
10 associated with said second plurality of transistors to suppress
11 phase-error between said in-phase and said quadrature-phase
12 signals.

17. The image rejecting down-converter as recited in Claim 15
2 wherein said inductor and said first capacitance resonate at twice
3 said frequency.

18. The image rejecting down-converter as recited in Claim 15
2 wherein said first capacitance is dominated by a base-to-emitter
3 capacitance of at least one of said plurality of transistors.

19. The image rejecting down-converter as recited in Claim 15
2 wherein said quadrature oscillator buffer further comprises a
3 capacitor, coupled to said inductor and coupled in parallel to said
4 current generator, said capacitor being configured to shunt said
5 inductor to ground at a selected RF.

20. The image rejecting down-converter as recited in Claim 15
2 wherein said frequency is at least three GHz.

21. The image rejecting down-converter as recited in Claim 15
2 where said in-phase and said quadrature-phase signals are four
3 periodic local oscillator signals having a 90 degree phase
4 difference.